Customer No.: 31561
Application No.: 10/064,206
Docket NO.: 08218-US-PA

REMARKS

Present Status of the Application

The disclosure is objected to because of the informalities on page 7, lines 17-19 of paragraph 21. Claims 5 and 11-20 are objected to because of some informalities. Claims 8, 14 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1-7, 9-13, 15-18 and 20 are allowable over prior art of record. Applicant has amended the specification and claims to overcome the objection. Applicant has also amended claims 8, 14 and 19 to improve clarity. Applicant has also added claims 21 and 22 to further define the invention. After entry of the foregoing amendments, claims 1-22 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of objections

Claims 5 and 11-20 are objected to because of some informalities. In response thereto, applicant has amended claims. The disclosure is objected to because of the informalities on page 7, lines 17-19 of paragraph 21. In response thereto, applicant has amended the disclosure by replacing the " AND gate (312)" with "decoder (304)", which is supported in Fig. 3 and also supported in the disclosure in lines 17-19 of paragraph 23, which stated "The decoding circuit (304) in the microprocessor

interface (302) derives a logic high state in the EN signal by referring the HCLK (as shown by a label 408) when there is no Zlen signal detected." The amendment is supported in the original specification and no new matter is entered. Reconsideration of those objections are respectfully requested

Discussion of Office Action Rejections

Claims 8, 14 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In response thereto, applicant has amended Claims 8, 14 and 19 to particularly point out and distinctly claim the subject matter. New claims 21 and 22 are added to further define the invention. Applicants respectfully traverse the rejections for at least the reasons set forth below.

More particularly, the language "two of the adjacent second address strobe signals are not continuously issued by the microprocessor interface" of claims 8 and 14 are deleted therefrom and the revised language "two of the adjacent second address strobe signals are not continuously issued by the microprocessor interface in two continuous cycles of the first clock" is respectively added to claims 21 and 22, and is also addressed to the amended claim 9. The amendment is supported by the disclosure in Paragraph [0024] as "two of the second ADS signals cannot be issued in two continuous HCLK cycles so that the second ADS signal can be maintained for a certain interval for circuit operations. Since the current bus specification employs logic low states on the

first ADS signal line for notifying a valid memory access demand, a logic high state should be kept for a certain interval between two adjacent first ADS signals for distinguishing purpose. Obviously, a continuous logic low state will not be used to indicate more than one first ADS signal because a logic low state can only indicate an active first ADS signal, which also implies that no two continuous second ADS signals occur in the embodiment."

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-22 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Belinda Lee

Belinda Lee
Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw